



N-Channel Reduced Q_g , Fast Switching MOSFET

CHARACTERISTICS

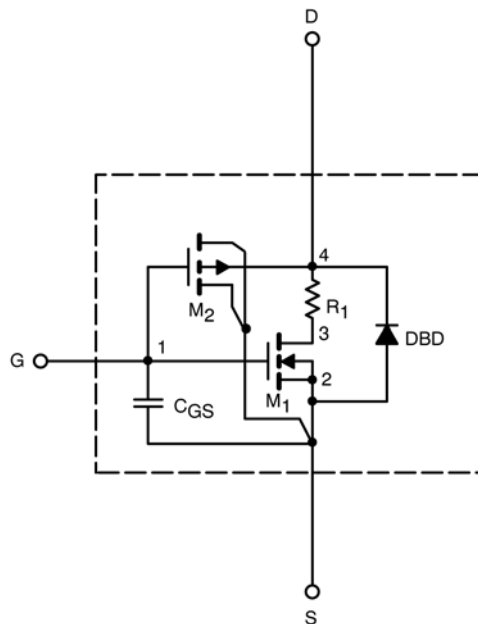
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model Si4850EY



Vishay Siliconix

SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Condition	Typical	Unit
Static				
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.95	V
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	248	A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 6 A	0.017	Ω
		V _{GS} = 10 V, I _D = 6 A, T _J = 125°C	0.026	
		V _{GS} = 10 V, I _D = 6 A, T _J = 175°C	0.032	
		V _{GS} = 4.5 V, I _D = 5.1 A	0.023	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 6 A	22	S
Diode Forward Voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	0.80	V
Dynamic^b				
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 6 A	17.5	nC
Gate-Source Charge	Q _{gs}		3.4	
Gate-Drain Charge	Q _{gd}		5.3	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω	22	ns
Rise Time	t _r		25	
Turn-Off Delay Time	t _{d(off)}		42	
Fall Time	t _f		48	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs	39	

Notes

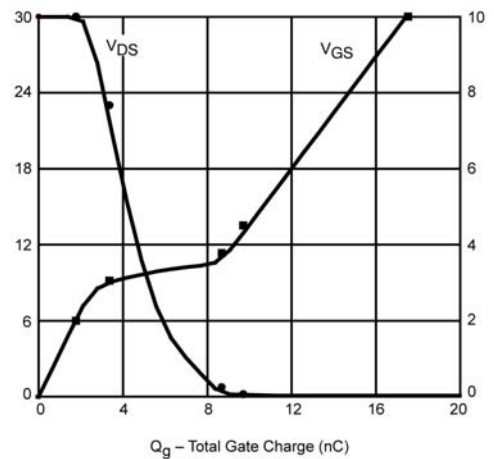
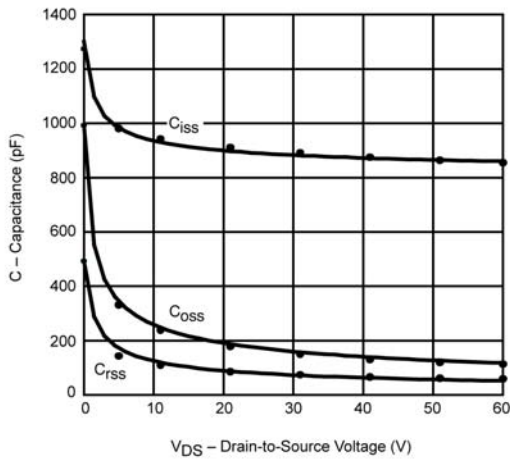
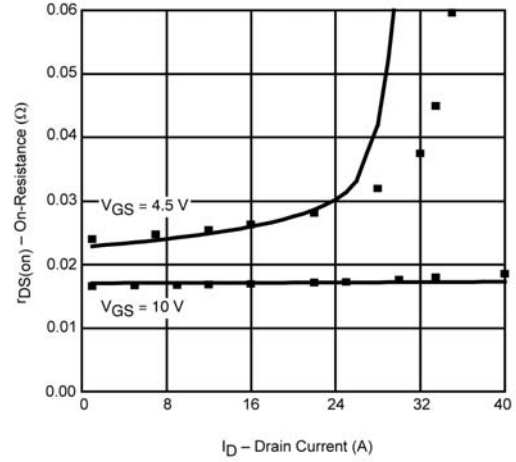
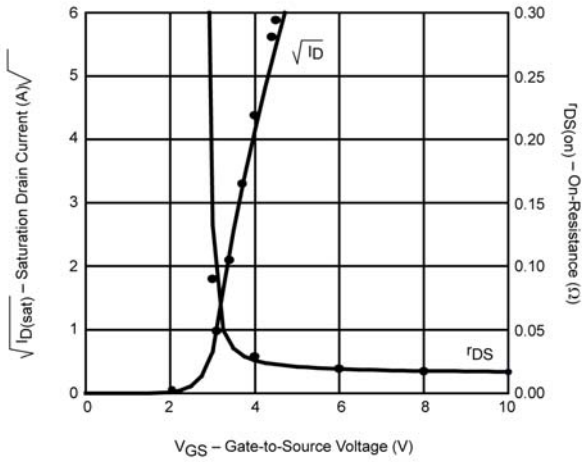
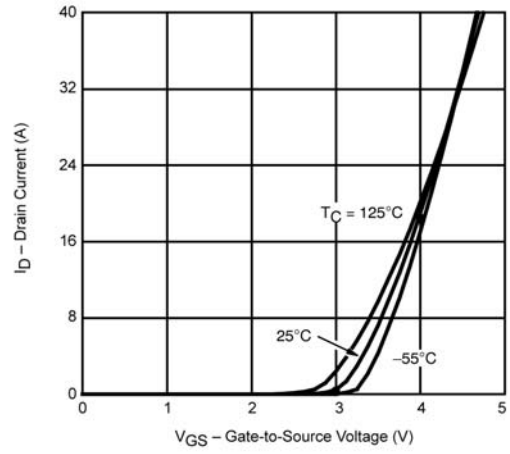
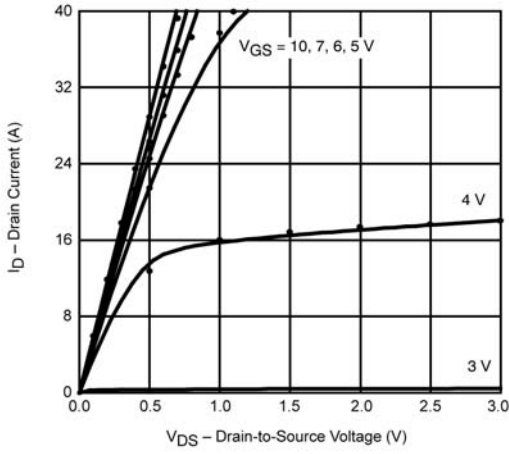
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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